

FIG. 1A (Prior Art)

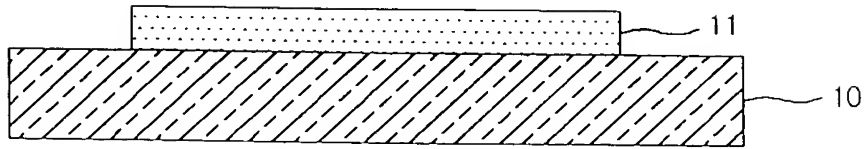


FIG. 1B (Prior Art)

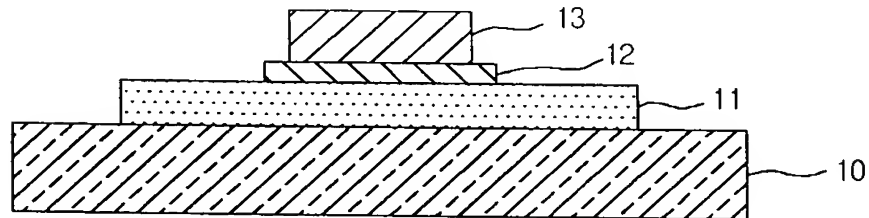


FIG. 1C (Prior Art)

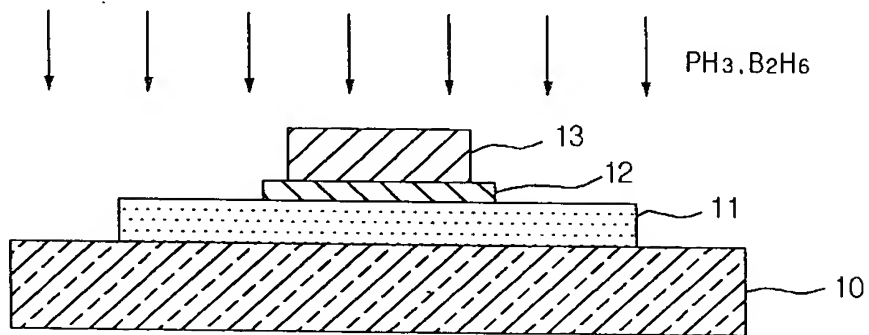
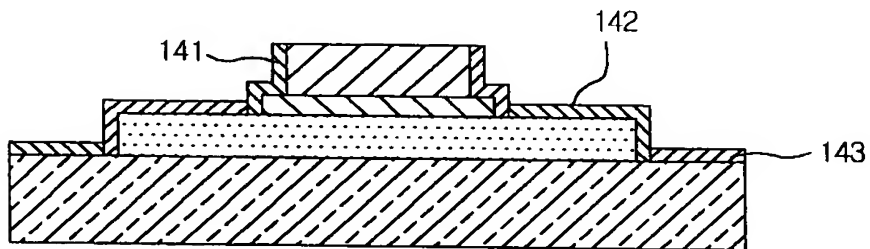


FIG. 1D (Prior Art)



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FIG. 1E (Prior Art)

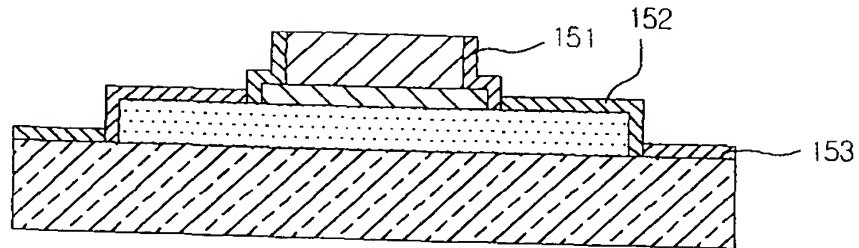


FIG. 1F (Prior Art)

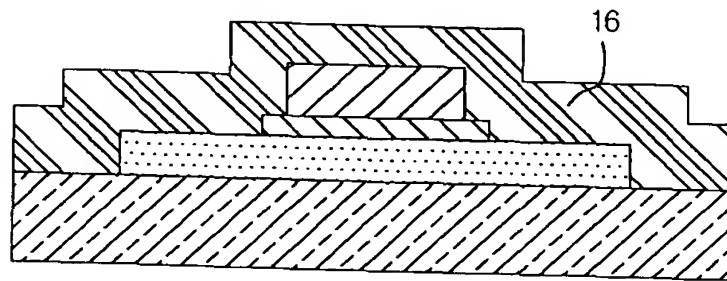
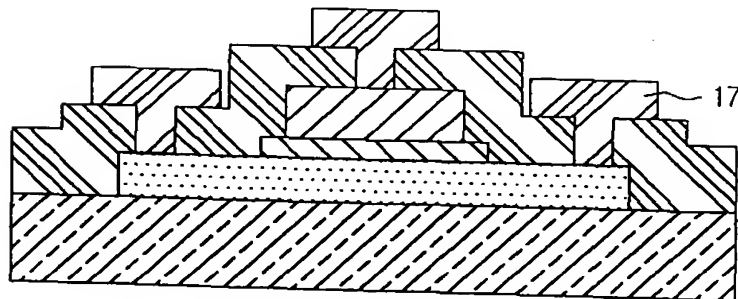


FIG. 1G (Prior Art)



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FIG. 2A

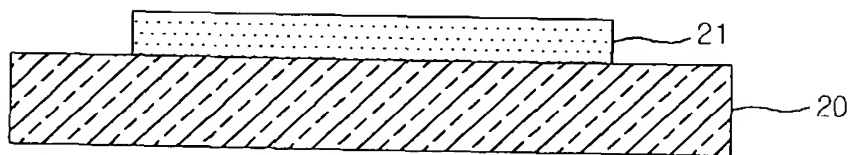


FIG. 2B

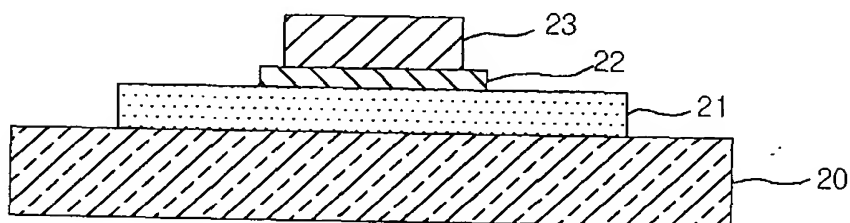
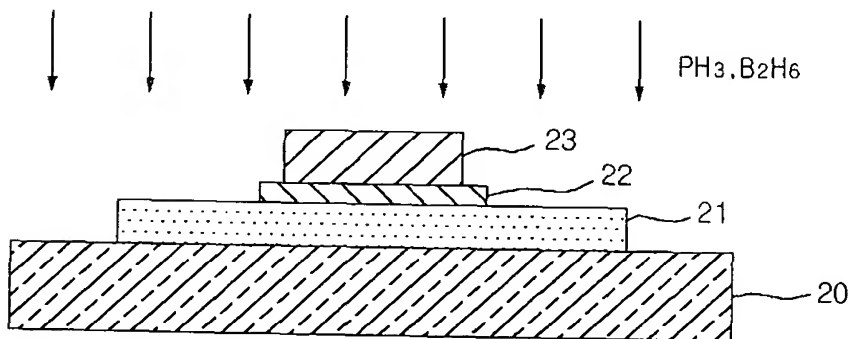


FIG. 2C



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A cross-sectional view of a semiconductor device. It shows a substrate 21 with a dashed pattern. On top of the substrate is a first conductive layer 22 with a dotted pattern. Above the first conductive layer is a second conductive layer 23 with a diagonal line pattern. On top of the second conductive layer is a third conductive layer 24 with a horizontal line pattern. A fourth conductive layer 25 is shown as a thin layer on top of the third conductive layer 24.

A cross-sectional view of a semiconductor device. It shows a substrate 22 with a diagonal hatching pattern. On top of the substrate is a first conductive layer 23 with a dotted pattern. A second conductive layer 24 with a diagonal hatching pattern is deposited on top of the first conductive layer 23. The second conductive layer 24 is thicker than the first conductive layer 23 and covers the entire top surface of the first conductive layer 23.

A cross-sectional view of a semiconductor device. It shows a substrate with diagonal hatching. On top of the substrate is a layer with a dotted pattern, labeled 26. Above this layer is a top layer with diagonal hatching, labeled 27. The top layer 27 has a stepped or patterned profile.

FIG. 3A

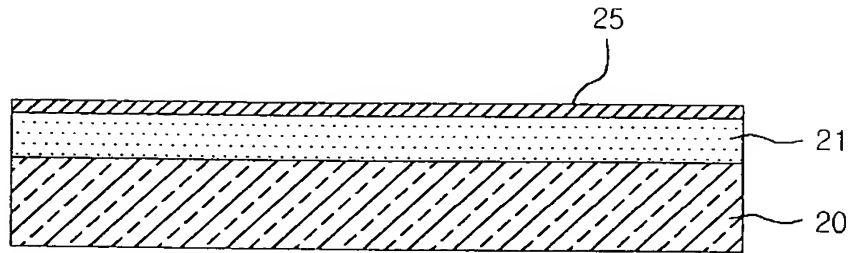


FIG. 3B

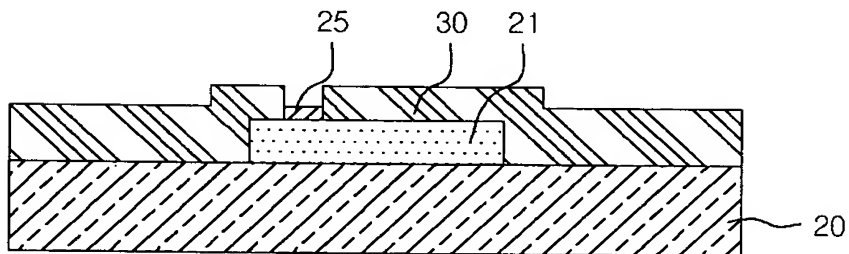


FIG. 3C

